

REMARKS

By the present Amendment, certain revisions have been made in the specification. More specifically, the values of elastic modulus of Comparative Examples 6 and 8 in Table 3 on page 32 have been amended from consistent with the description provided with respect to Comparative Preparation Examples 6 and 8 on page 28, lines 3-4 and 29-30, respectively.

The present Amendment also amends claim 1 to define one aspect of the present invention with greater precision. In particular, claim 1 has been amended so that the surface protecting adhesive film is defined as being an acrylic adhesive layer having a storage elastic modulus from 1×10^5 Pa to 1×10^7 Pa at 150 °C and as having an adhesive force of from 5 g/25 mm to 500 g/25mm in terms of an adhesive strength in regard to an SUS304-BA plate. The recitation of an acrylic adhesive layer is supported by the description provided in the paragraph starting at page 6, line 11 and the Examples as illustrated by the description on page 18, lines 1-18. The adhesive force recitation is supported by the specification by the passage set forth on page 12, lines 17 to 19. The recitation of the adhesive strength provides good peeling workability in a step of peeling a surface protecting adhesive film from the semiconductor wafer where adhesive residue can provide a problem.

The present Amendment also amends claim 3 to place the claim in independent form based on the original recitations of claim 1. Claim 3 and claim 4 which depends therefrom are fully supported by Japanese priority application no 2002-090493, filed on March 28, 2002, as can be determined by review of the attached verified English translation thereof. The significance of this submission will be explained below concerning the rejection of claims 3 and 4.

As explained in greater detail in the specification, the present invention can provide substantial advantages. In particular, the defined surface protecting adhesive film can enable the back surface of a semiconductor wafer to be effectively ground and a damaged layer removed while protecting the wafer from breakage. Furthermore, the adhesive film can be removed from the processed wafer without leaving an adhesive residue. Such advantageous results can be understood by considering the Examples and results in Tables 1 and 2 on pages 30 and 31. In sharp contrast, when an adhesive film is prepared which does not follow the teachings of the present invention, as shown in the Comparative Examples of Table 3 on page 32, the wafer can be cracked, broken or deformed and/or adhesive residue can be present.

With a clear understanding of the present invention, as defined by the claims of record, and supported by the technical evidence provided in the specification, those of ordinary skill in the art will recognize that the cited documents do not disclose or teach the present invention and certainly do not appreciate the noted advantageous results which can be obtained therefrom. Nagai et al., U.S. Pat No. 6,114,753, discloses a semiconductor device, comprising a semiconductor element, a circuit tape having a circuit layer, external terminals for electrically connecting the circuit tape to a mounting substrate and an adhesive film for adhering the circuit tape to the semiconductor element such that the semiconductor element is insulated from the circuit tape, wherein the circuit layer is connected to a pad of the semiconductor element and the external terminal, and an elastic modulus of the adhesive film in a temperature region of 200° -250° C. is more than 1 MPa. The film material is used as the body for buffering the thermal stress generated by the difference in thermal expansion between the mounting substrate and the semiconductor element and the

resulting semiconductor device is said to have superior connection reliability by providing a buffer body for absorbing the difference of thermal expansion between the mounting substrate and the semiconductor element in a semiconductor package structure, even if an organic material is used for the mounting substrate.

Those of ordinary skill in the art will fully understand that the film material of Nagai et al. is used for an entirely different purpose than the surface protecting film of the present invention. The disclosed film material is specifically designed to hold portions of a semiconductor device together and to provide a buffer body to protect against the problems associated with thermal expansion. The disclosed film material of Nagai et al. has nothing to do with protecting a semiconductor wafer during grinding and further processing and then being removable so as to avoid an adhesive residue. Quite to the contrary, the disclosed film material is used for the purpose of to hold portions of the semiconductor element together. Accordingly, the disclosed adhesive layer does not meet the claimed adhesive force "from 5g/25mm to 500g/25mm in regard to an SUS304-BA plate whereby the acrylic adhesive layer can be peeled away from a semiconductor wafer surface". Furthermore, given the distinct function of the adhesive layer of Nagai et al., it would be contrary to the intended purpose of such adhesive layer of to even attempt to modify it in accordance with the adhesive force of claim 1. This understanding is supported from the description of Nagai et al. that a characteristic of "delamination" is evaluated as a negative property (see column 9, lines 43-44 where delamination is referred to as a "defect"). Accordingly, Nagai et al. cannot be used to reject claims 1 and 2 of the present application.

Turning to the rejection of claims 3 and 4, the Examiner has relied on the combination of Nagai et al. with Takyu et al., U.S. Patent No. 6,699,774 and Inuzuka

et al., U.S. Patent No. 6,777,310, with the latter two patents being used to allegedly show the method recited in claim 3. Applicants submit that the proposed combination of patents is without proper foundation since the designed purpose of the film material of Nagai et al. is distinct from the tapes of the other patents. As pointed out above, Nagai et al. acknowledges the problem of delamination while the tapes of Takyu et al. and Inuzuka et al. are designed to be removed from the semiconductors as shown by the passage in Inuzuka et al. at column 5, lines 58-62. Indeed, absent improper resort to applicants' own specification, those of ordinary skill in the art would not even attempt to make the hypothetical combination of patents set forth in the Official Action. Moreover, the cited patents do not in any way appreciate the substantial advantages which can be obtained in accordance with the present invention which are clearly shown in the specification.

A further reason why claims 3 and 4 cannot be rejected based on the noted patents is that Takyu et al. and Inuzuka et al. are not "prior art" against the claims of the present application. Each of these patents has a U.S. filing date which is after the above-mentioned Japanese priority date of March 28, 2002, that is claimed in the present application. It will be noted from the attached English translation of the priority application that claims 3 and 4 parallel original claims 3 and 4 of the present application. The storage elastic modulus originally recited in claim 1 of the present application and now incorporated into claim 3 is described in claim 1 of the priority application as well as paragraph [0017]. Therefore, since Takyu et al. and Inuzuka et al. are not "prior art", the rejection of claims 3 and 4 in part relying on these patents, cannot stand.

For all of the reasons set forth above, applicants respectfully submit that the claims of record are patentable over the cited prior art and therefore request

reconsideration and allowance of the present application. Applicants also note that an Information Disclosure Statement was filed on July 20, 2005, and request that an acknowledged citation form be returned with the next Official Action.

Should the Examiner wish to discuss any aspect of the present application, he is invited to contact the undersigned attorney at the number provided below.

Respectfully submitted,

BUCHANAN INGERSOLL PC

By: Robert G. Mukai
Robert G. Mukai
Registration No. 28,531

P.O. Box 1404
Alexandria, Virginia 22313-1404
(703) 836-6620

Date: November 1, 2005